WHAT IS CLAIMED IS:

1. A trench isolation method for forming a semiconductor device comprising:

forming an etching mask pattern on a semiconductor substrate to expose a predetermined region of the semiconductor substrate;

etching the exposed semiconductor substrate, using the etching mask pattern as an etching mask, to form a trench;

forming an insulating layer over the trench and nearby regions, the insulating layer filling the trench;

providing a material layer on the insulating layer, the material layer being formed at a temperature of 500°C and higher;

planarly etching the material layer and the insulating layer down to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench; and

removing the exposed etching mask pattern.

2. The method of Claim 1, wherein the insulating layer is selected from a group of materials consisting of high density plasma (HDP) oxide or undoped silicate glass (USG).

3. The method of Claim 1, wherein the material layer consists of one selected from a group consisting of high temperature oxide (HTO), high temperature USG, polysilicon, and amorphous silicon.

4. The method of Claim 1, wherein forming the etching mask pattern includes:

forming a pad oxide layer on the semiconductor substrate;

forming an etch-stop layer on the pad oxide layer; and

patterning the etch-stop layer and the pad oxide layer to expose the predetermined region of the substrate.

5. The method of Claim 4, wherein the pad oxide layer is formed to a thickness of 20Å~200Å.

6. The method of Claim 4, wherein the etch-stop layer comprises silicon nitride with a thickness of 500Å~2000Å.

7. The method of Claim 4, wherein the etch-stop layer comprises a polysilicon layer and an HTO layer which are sequentially stacked.

8. The method of Claim 1 further comprising, prior to forming the insulating layer:

forming an oxide layer on an inner wall and bottom of the trench; and

forming an oxidation barrier layer on the oxide layer.

9. The method of Claim 8, wherein the oxide layer comprises thermal oxide or chemical vapor deposition (CVD) oxide with a thickness of 20Å~300Å.

10. The method of Claim 8, wherein the oxidation barrier layer comprises silicon nitride with a thickness of 20Å~300Å.

11. The method of Claim 8 further comprising forming a capping layer between the oxidation barrier layer and the insulating layer.

12. The method of Claim 11, wherein the capping layer is made of CVD oxide with a thickness of 20Å~300Å.